IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jong Chan	Examiner: Unknown
Serial No.:	Unknown (Parent Serial No.: 09/085,204)	Group Art Unit: Unknown
Filed:	Herewith (Parent Filing Date: May 27, 1998)	Docket No.: 10980422-3
Title:	MEMORY CONTROLLER SUPPORTING REDUNDANT SYNCHRONOUS MEMORIES	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir/Madam:

This Preliminary Amendment is filed concurrent with the Divisional Patent Application filed on even date herewith. Please amend the above-identified application as follows:

IN THE SPECIFICATION

Please replace the paragraph beginning at page 15, line 7, with the following rewritten paragraph:

Fig. 6 illustrates the memory bus 230 and bus switches 290, 292, and 294 in each I/O control logic unit 212. Each memory bus 230 is composed of a number of signal paths (i.e., lines or traces) that carry address, data, and control signals. The address signals 266 are generated by the memory controller 224. The data signals 225 are received from the PCI bus 228. The control signals includes a local memory select signal 262, a remote memory select signal 264, and a read/write control signal 268A.

IN THE CLAIMS

Please cancel claims 1-36 without prejudice.

Please add new claims 37-48 as follows:

37. A method for controlling a transfer of data between a data processor and a data unit, the method comprising: